JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech. Degree COURSE STRUCTURE in

EMBEDDED SYSTEMS

I YEAR - I Semester

Code	Group	Subject	L	P	Credits
		Microcontrollers for Embedded System Design	3	0	3
		Embedded Real Time Operating Systems	3	0	3
		VLSI Technology & Design	3	0	3
		Advanced Computer Networks	3	0	3
	Elective -I	Advanced Computer Architecture	3	0	3
		Wireless LANs & PANs			
		Advanced Digital Signal processing			
	Elective -II	Digital System Design	3	0	3
		Neural Networks & Applications			
		Advanced Operating Systems			
	Lab	Embedded Systems Lab - I	0	3	2
		Seminar	-	-	2
		Total Credits (6 Theory + 1 Lab.)			22

I Year – I Sem. M.Tech (Embedded Systems)

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Unit – I: Introduction to Embedded Systems
Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, Classification of Embedded Systems.

Unit – II: Microcontrollers and Processor Architecture & Interfacing
8051 Architecture, Input/Output Ports and Circuits, External Memory, Counters and Timers, PIC Controllers. Interfacing Processor (8051, PIC), Memory Interfacing, I/O Devices, Memory Controller and Memory arbitration Schemes.

Unit – III: Embedded RISC Processors & Embedded System-on Chip Processor
PSOC (Programmable System-on-Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC, Embedded RISC Processor architecture – ARM Processor architecture, Register Set, Modes of operation and overview of Instructions

Unit – IV: Interrupts & Device Drivers
Exceptions and Interrupt handling Schemes – Context & Periods for Context Switching, Deadline & interrupt latency. Device driver using Interrupt Service Routine, Serial port Device Driver, Device drivers for Internal Programmable timing devices

Unit – V: Network Protocols
Serial communication protocols, Ethernet Protocol, SDMA, Channel & IDMA, External Bus Interface

TEXT BOOKS:

1. Embedded Systems - Architecture Programming and Design – Raj Kamal, 2nd ed., 2008,TMH.
2. PIC Microcontroller and Embedded Systems – Muhammad Ali Mazidi, Rolin D.Mckinaly, Danny Causy – PE.
3. Designers Guide to the Cypress PSOC – Robert Ashpy, 2005, Elsevier.

REFERENCES:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.
2. ARM Systems Developers Guides- Design & Optimizing System Software - Andrew N. Sloss, Dominic Symes, Chris Wright, 2004, Elsevier.
3. Designing with PIC Microcontrollers- John B. Peatman, 1998, PH Inc.

I Year – I Sem. M.Tech (Embedded Systems)

EMBEDDED REAL TIME OPERATING SYSTEMS

Unit – I: Introduction
Introduction to UNIX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec), Signals, Interprocess communication,(pipes, fifos, message queues, semaphores, shared memory)

Unit II: Real Time Systems:
Typical real time applications, Hard Vs Soft real-time systems, A reference model of Real Time Systems: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

Unit III: Scheduling & Inter-process Communication
Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs Online Scheduling.
Inter-process Communication and Synchronization of Processes, Tasks and Threads- Multiple Process in an Application, Problem of Sharing data by multiple tasks & routines, Inter-process communication

Unit IV: Real Time Operating Systems & Programming Tools
Operating Systems Services, I/O Subsystems, RT & Embedded Systems OS, Interrupt Routine in RTOS Environment
Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of µCOS-II

Unit V: VX Works & Case Studies
Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches-semaphore- Binary mutex, counting watch dugs, I/O system
Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using µCOS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

TEXT BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2nd ed., 2008,TMH.
2. Real Time Systems- Jane W. S. Liu- PHI.
3. Real Time Systems- C.M.Krishna, KANG G. Shin, 1996, TMH

REFERENCES:

1. Advanced UNIX Programming, Richard Stevens
2. VX Works Programmers Guide

I Year – I Sem. M.Tech (Embedded Systems)

VLSI TECHNOLOGY & DESIGN

UNIT – I:
Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends And Projections.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds}-V_{ds} relationships, Threshold Voltage V_t, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:
LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT – III:
COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – V:
FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS:
1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.

REFERENCES:
1. Principals of CMOS VLSI Design – N.H.E Weste, K.Eshraghian, 2nd ed., Adisson Wesley.

I Year – I Sem. M.Tech (Embedded Systems)

ADVANCED COMPUTER NETWORKS

Unit -I: Congestion and Quality of Service (QoS)
Data traffic, Congestion, Congestion Control, Open loop and Closed Loop Congestion Control in TCP and Frame Relay, Quality of Service, Flow Characterization, Flow Classes, Need For QoS, Resource Allocation, Best Effort Service Features, Techniques to Improve QoS.
Queue Management: Passive, Active (RED), and Fair (BRED, Choke) Queue Management Schemes, Scheduling, Traffic Shaping, Resource Reservation and Admission Control Scheduling, Integrated and Differential Services.

Unit-II:
Wireless Local Area Networks: Introduction, Wireless LAN Topologies, Wireless LAN Requirements, the Physical Layer, the Medium Access Control (MAC) Layer, Latest Developments.
Wireless Personal Area Networks (WPANs): Introduction to PAN Technology and Applications, Commercial Alternatives- Bluetooth, Home RF.
Wireless Wide Area Networks and MANS: The Cellular Concept, Cellular Architecture, The First-Generation Cellular Systems, The Second- Generation Cellular Systems, The Third- Generation Cellular Systems, Wireless in Local Loop, Wireless ATM, IEEE 802.16 Standard.

Unit-III:
Cellular Systems and Infrastructure- Based Wireless Networks: Cellular Systems Fundamentals, Channel Reuse, SIR and User Capacity, Interference Reduction Techniques, Dynamic Resource Allocation, Fundamental Rate Limits.
Virtual Private Network (VPN): Types of VPN, VPN General Architecture, Current VPN Advantages and Disadvantages, VPN Security Issues, VPN Standards.

Unit-IV:
ATM Protocol Reference Model: Introduction, Transmission Convergence (TC) Sub-layer, Physical Medium Dependent (PMD) Sub-layer, Physical Layer Standards for ATM.
ATM Layer: ATM Cell Header Structure at UNI, ATM Cell Header Structure at NNI, ATM Layer Functions.
ATM Adaptation Layer: Service Classes and ATM Adaptation Layer, ATM Adaptation Layer 1 (AAL1), ATM Adaptation Layer 2 (AAL2), ATM Adaptation Layer 3/4 (AAL3/4), ATM Adaptation Layer 5 (AAL5).
ATM Traffic and Service Parameterization: ATM Traffic Parameters, ATM Service Parameters, Factors Affecting QoS Parameters, ATM Service Categories, QoS and QoS Classes.

Unit-V:
Interconnection Networks: Introduction, Banyan Networks- Properties, Crossbar Switch, Three Stage Class Networks, Rearrangeable Networks, Folding Algorithm, Benes Networks, Looping Algorithm, Bit- Allocation Algorithm.
SONET/SDH: SONET/SDH Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks.

TEXT BOOKS:

1. Wireless Communications - Andrea Goldsmith, 2005, Cambridge University Press.
2. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
3. Data Communication and Networking - B. A.Forouzan, 2nd updating, 2004,TMH

REFERENCES:

1. Introduction to Broadband Communication Systems- Sadiku, Mathew N.O., Akujuobi, Cajetan.M, PHI
2. Wireless Networks- P. Nicopolitidis, A. S. Pomportsis, G. I. Papadimitriou, M. S. Obaidat, 2003, JohnWiley & Sons
3. High Performance TCP / IP Networking – Mahaboob Hassan, Jain Raj, PHI.
4. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

I Year – I Sem. M.Tech (Embedded Systems)

ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE – I)

UNIT I

Concept of instruction format and instruction set of a computer, types of operands and operations; addressing modes; processor organization, register organization and stack organization; instruction cycle; basic details of Pentium processor and power PC processor, RISC and CISC instruction set.

UNIT II

Memory devices; Semiconductor and ferrite core memory, main memory, cache memory, associative memory organization; concept of virtual memory; memory organization and mapping; partitioning, demand paging, segmentation; magnetic disk organization, introduction to magnetic tape and CDROM.

UNIT III

IO Devices, Programmed IO, interrupt driver IO, DMA IO modules, IO addressing; IO channel, IO Processor, DOT matrix printer, ink jet printer, laser printer.

Advanced concepts; Horizontal and vertical instruction format, microprogramming, microinstruction sequencing and control; instruction pipeline; parallel processing; problems in parallel processing; data hazard, control hazard.

UNIT IV

ILP software approach-complier techniques-static branch protection-VLIW approach-H.W support for more ILP at compile time-H.W verses S.W solutions

Multiprocessors and thread level parallelism-symmetric shared memory architectures-distributed shared memory-Synchronization-multi threading.

UNIT V

Storage System-Types-Buses-RAID-errors and failures-bench marking a storage device designing a I/O system.

Inter connection networks and clusters-interconnection network media – practical issues in interconnecting networks-examples-clusters-designing a cluster

Text Books:

1. "Computer organization and architecture", Williams Stallings, PHI of India, 1998.
2. Computer organization, Carl Hamachar, Zvonko Vranesic and Safwat Zaky, McGraw Hill International Edition.
3. Computer Architecture & Organization, John P. Hayes, TMH III Edition.
4. Computer Architecture A quantitative approach 3rd edition John L. Hannessy & David A. Patteson Morgan Kufmann (An Imprint of Elsevier)

Reference Books:

1. "Computer Architecture and parallel Processing" Kai Hwang and A. Briggs International edition McGraw-Hill.
2. Advanced Computer Architecture, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson.

I Year – I Sem. M.Tech (Embedded Systems)

WIRELESS LANS AND PANS
(ELECTIVE – I)

UNIT 1: Overview of Wireless Communication

History of wireless communication, Wireless Vision, Technical Issues, Surrent Wireless Systems, The Wireless Spectrum.

Unit 2: Introduction to Wireless LANS

Historical Overview of LAN Industry, Evolution of The WLAN Industry, Wireless Home Networking, WLAN Application, WLAN Components, WLAN Modes, WLAN Standards and operation.

Unit 3: High-speed Wireless LANs and WLAN Security

IEEE 802.11a and IEEE 802.11b and other WLAN Standards, WLAN Security.

Unit 4: Low Rate Wireless Personal Area Networks

Infrared WPANs, RFWPANs, Low rate WPAN Security, High rate WPAN Standards, 802.15.3, High rate WPANs, Ultra Wideband, WPAN Challenges.
Wireless Wide Area Networks: Cellular Telephone Applications, Digital Cellular Technology, Client Software, Digital Cellular Challenges and Outlook, Satellite Broadband Wireless.
Wireless Metropolitan Area Networks: What is WMAN?, Land- Based Fixed Broadband Wireless, IEEE 802.16 (WiMAX), WMAN Security.

Unit 5: Ad-Hoc- Wireless Networks

Application, Design Principles and Challenges, Protocol Layers, Cross Layer Design, Network Capacity Limits, Energy Constrained Networks. Cellular and Adhoc wireless networks, applications, MAC protocols, Routing, Multicasting, Transport layer Protocols, quality of service browsining, deployment considerations, Adhoc wireless Internet.

TEXT BOOKS:

1. Wireless Communication- Andrea Goldsmith, Cambridge University Press.
2. Wireless Communication- Marks Ciampor, Jeorge Olenewa, 2007, Cengage Learning.
3. Wireless Networks- Kaveh Pahlaram, Prashant Krishnamurthy, 2002, PHI.

I Year – I Sem. M.Tech (Embedded Systems)

ADVANCED DIGITAL SIGNAL PROCESSING
(ELECTIVE – I)

UNIT I
Review of DFT, FFT, IIR Filters, FIR Filters,
Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT II
Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT III
Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT –IV
Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT V
Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis & D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3. DSP – A Pratical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCES:

1. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
2. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
3. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

I Year – I Sem. M.Tech (Embedded Systems)

DIGITAL SYSTEM DESIGN
(ELECTIVE – II)

Unit-I: Designing with Programmable Logic Devices
Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA's– Using a One-hot state assignment,
State transition table- State assignment for FPGA's - Problem of Initial state assignment for One –Hot encoding - State Machine charts – Derivation of SM Charts – Realization of SM charts – Design Examples – Serial adder with Accumulator - Binary Multiplier – Signed Binary number multiplier (2's Complement multiplier) – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL.

Unit-II: Fault Modeling & Test Pattern Generation
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model
Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Unit-III: Fault Diagnosis in Sequential Circuits
Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Unit-IV: PLA Minimization and Testing
PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-V: Minimization and Transformation of Sequential Machines
The Finite state Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.
Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCES:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

I Year – I Sem. M.Tech (Embedded Systems)

NEURAL NETWORKS AND APPLICATIONS
(ELECTIVE – II)

UNIT – I Fundamental Concepts, Models & Learning Rules of Artificial Neural Systems
Biological Neuron Models and their Artificial Models Biological Neuron, McCulloch-Pitts Neuron Model, Neuron Modeling for Artificial Neuron Models, Models of Artificial Neural Networks; Feed Forward Network and Feed Backward Network. Neural Processing, Supervised and Unsupervised Learning

Neural Network Learning rules: Hebbian Learning Rule, Perception Learning Rule, Delta Learning Rule Widrow-Hoff Rule, Correlation Learning Rule, Winner –Take-All Learning Rule, Out Star Learning Rule, Summary of Learning Rules.

UNIT – II Single Layer Feed Forward Networks
Classification Model, Features and Decision Regions, Discriminant Functions, Linear Machine and Minimum Distance Classification, Nonparametric Training Concept, Training and Classification using the Discrete Perceptron: Algorithm and Examples. Single Layer Continuous Perceptron Networks for Linearly Separable Classifications, Perceptron Convergence Theorem, Multicategory Single Layer Perceptron Networks.

UNIT – III Multilayer Feed Forward Networks

Linearly Nonseparable Pattern Classification, Delta Learning Rule for Multiperception layer. Generalized Delta Learning Rule. Feed Forward Recall and Error Back Propagation Training; Examples of Error Back-Propagation, Training Errors, Learning Factors; Initial weights Cumulative Weight Adjustment versus Incremental Updating, Steepness of activation function, learning constant, momentum method, Network architecture Versus Data Representation, Necessary number of Hidden Neurons. Application of Back propagation Networks in pattern recognition & Image processing

UNIT – IV Associative Memories
Basic concepts Linear associator ,Basic concepts of Dynamical systems. Mathematical Foundation of Discrete-Time Hop field Networks. Mathematical Foundation of Gradient-Type Hopfield Networks. Transient response of Continuous Time Networks. Example Solution of Optimization Problems; Summing networks with digital outputs. Minimization of the Traveling salesman tour length, Solving Simultaneous Linear Equations. Boltzman machines,Bidirectional Associative Memory; Multidirectional Associative Memory. Associative Memory of Spatio-temporal Patterns

UNIT – V Matching And Self-Organizing Networks
Hamming net and MAXNET Unsupervised learning of clusters. Clustering and similarity measures Winner take all learning ,recall mode, initialization of weights, separability limitations. Counter propagation networks. feature mapping: Self organizing feature maps. Cluster discovery networks (ART1).

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.

REFERENCES:

1. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International
2. Artificial Neural Network –Simon Haykin, 2nd ed., Pearson Education
3. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.
4. Fundamental of Neural Networks –Laurene Fausett

I Year – I Sem. M.Tech (Embedded Systems)

ADVANCED OPERATING SYSTEMS
(ELECTIVE – II)

Unit – I:

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

Unit – II:

Introduction to UNIX and LINUX: Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations

Unit – III:

System Calls: System calls and related file structures, Input / Output, Process creation & termination.

Inter process Communication: Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

Unit – IV:

Introduction to Distributed systems: Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

Unit – V:

Synchronization in Distributed systems : Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The design of the UNIX Operating Systems – Maurice J.Bach,1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete reference LINUX – Richard Peterson, 4th ed., McGraw – Hill.

REFERENCES:

1. Operating Systems : Internal and Design Principles - Stallings, 6th ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum 3rd ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th ed.,, John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens ,1998, PHI.
6. The UNIX Programming Environment – Kernighan & Pike, PE.

I Year – I Sem. M.Tech (Embedded Systems)

EMBEDDED SYSTEMS LAB-1

CYCLE 1: 8051 Microcontrollers

1. Serial Data Transmission using 8051 microcontroller in different modes.
2. Look up tables for 8051.
3. Timing subroutines for 8051- Real time times and Applications.
4. Keyboard interface to 8051.
5. ADC, DAC interface to 8051.
6. LCD interface to 8051.

CYCLE 2:

1. Study of Real Time Operating Systems.
2. Development of Devices Drivers for RT Linux.
3. Software Development for DSP Applications.
4. Serial Communication Drivers for ARM Processors.
5. Case Studies- Any two

a. Design of RTOS Kernel.
b. Cross Compiler/ Assembler.
c. Vx Works.