JYOTHISHMATHI INSTITUTE OF TECHNOLOGY AND SCIENCE

TOPIC: Combinational Circuits

Sub: Switching Theory and Logic Design

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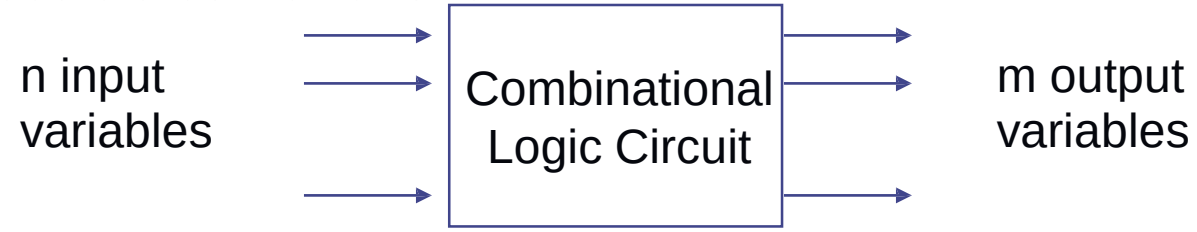
Combinational Circuits

- A combinational circuits with n of input values
  - 2^n possible combinations



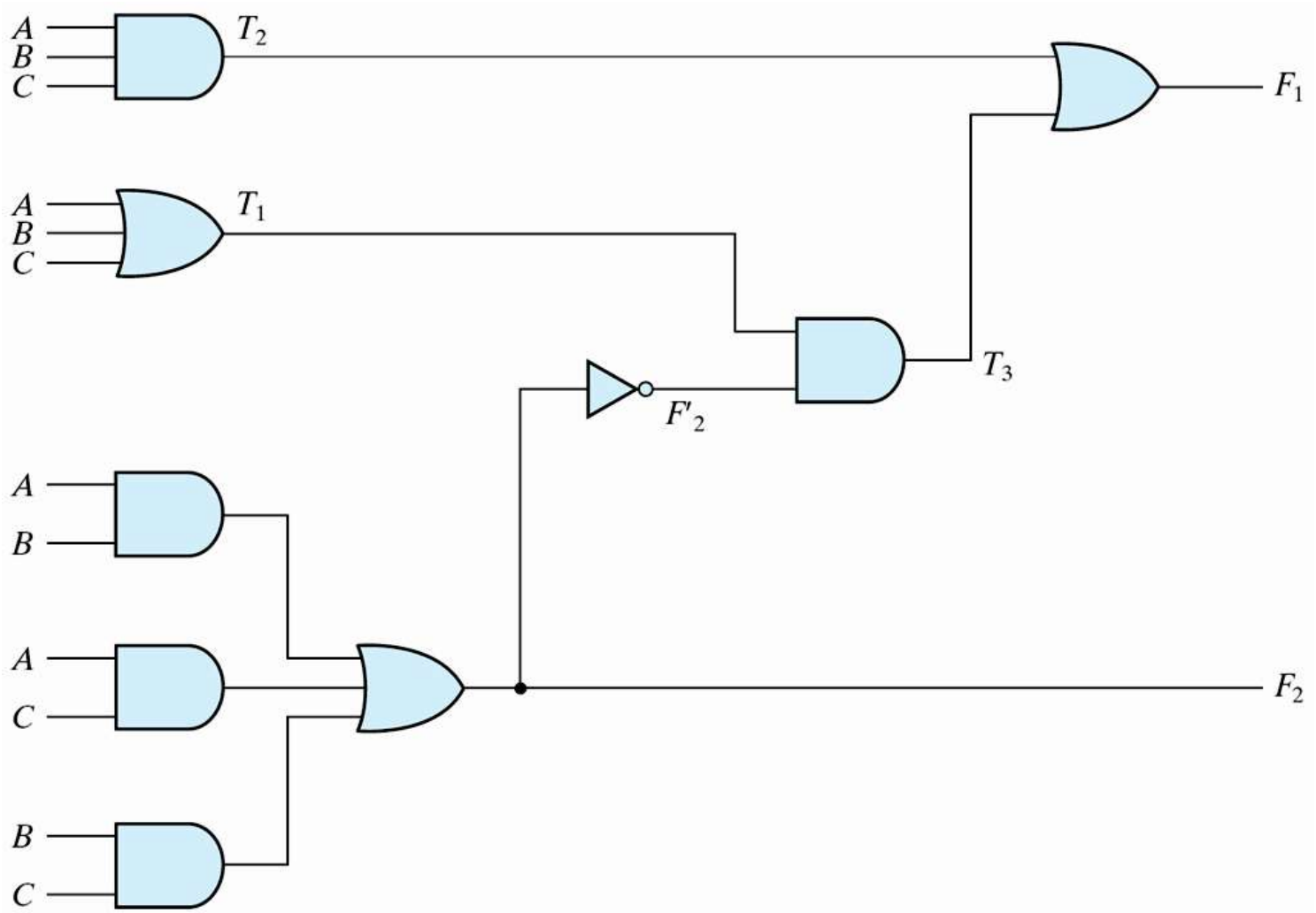
  - Specific functions
    - Adders, subtractors, comparators, decoders, encoders, and multiplexers
      - MSI circuits or standard cells

Analysis Procedure

- Step 1: Label all gate outputs that are a function of input variables with arbitrary symbols – but with meaningful names. Determine the Boolean functions for each gate output.
- Step 2: Label the gates that are a function of input variables and previously labeled gates with other arbitrary symbols. Find the Boolean functions for these gates.
- Step 3: Repeat the process outlined in step 2 until the outputs of the circuit are obtained.
- Step 4: By repeated substitution of previously defined functions, obtain the output Boolean functions in terms of input variables.

Analysis Procedure Example

- A straight-forward procedure



Analysis Procedure Example

- Step 1:
  - F_2 = AB+AC+BC
  - T_1 = A+B+C
  - T_2 = ABC
- Step 2:
  - $T_3 = F_2'T_1$
- Step 3:
  - $F_1 = T_3+T_2$
- Step 4:
  - $F_1 = T_3+T_2 = F_2'T_1+ABC$
    = (AB+AC+BC)'(A+B+C)+ABC
    = (A'+B')(A'+C')(B'+C')(A+B+C)+ABC
    = (A'+B'C')(AB'+AC'+BC'+B'C)+ABC
    = A'BC'+A'B'C+AB'C'+ABC

Truth Table

Table 4.1
Truth Table for the Logic Diagram of Fig. 4.2

A	B	C	F_2	F_2'	T_1	T_2	T_3	F_1
0	0	0	0	1	0	0	0	0
0	0	1	0	1	1	0	1	1
0	1	0	0	1	1	0	1	1
0	1	1	1	0	1	0	0	0
1	0	0	0	1	1	0	1	1
1	0	1	1	0	1	0	0	0
1	1	0	1	0	1	0	0	0
1	1	1	1	0	1	1	0	1

Decoder

- An *n*-to-*m* decoder
  - a binary code of *n* bits = 2^n distinct information
  - *n* input variables; up to 2^n output lines
  - only one output can be active (high) at any time

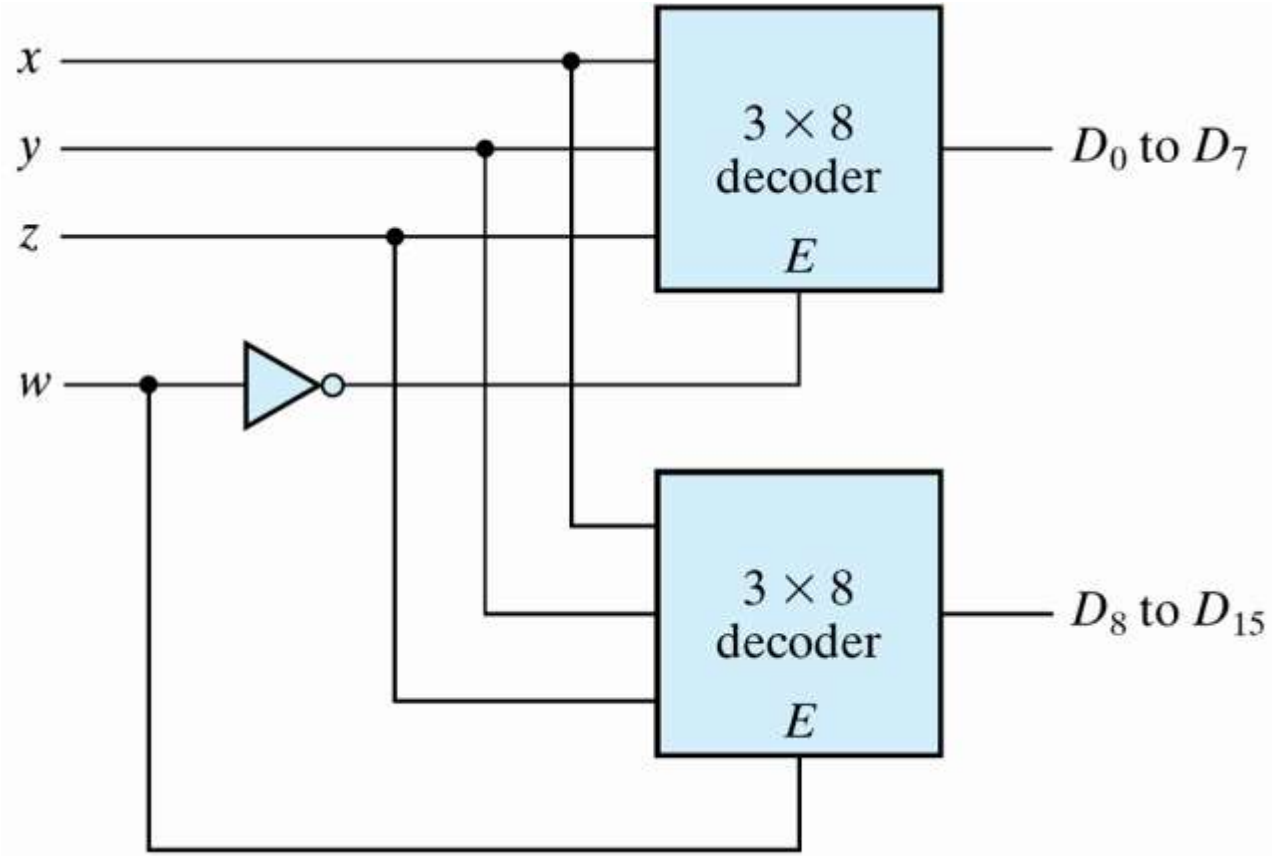
Table 4.6

Truth Table of a Three-to-Eight-Line Decoder

Inputs			Outputs							
x	*y*	*z*	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

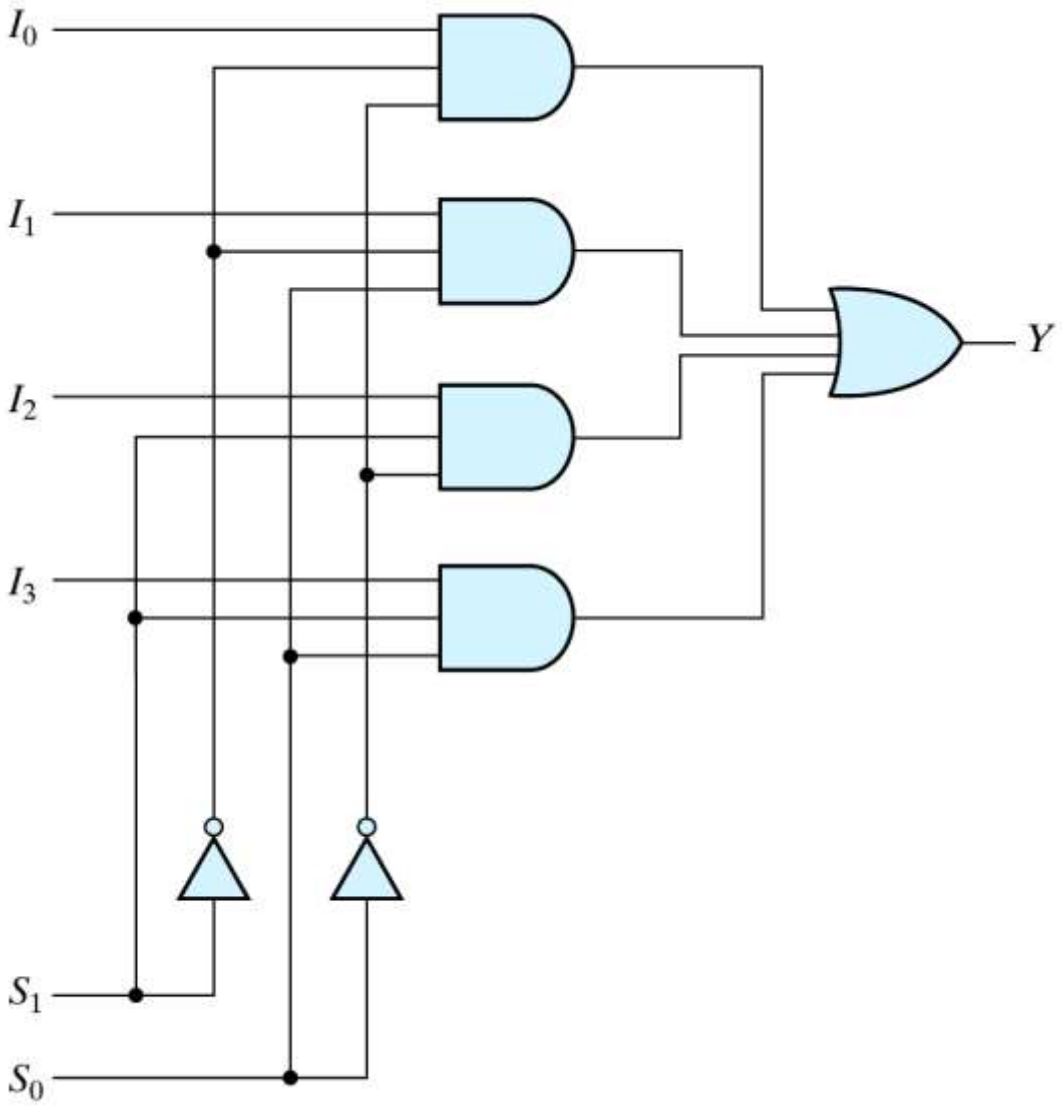
4x16 Decoder

- Expansion
  - two 3-to-8 decoder: a 4-to-16 decoder



4 × 16 decoder constructed with two 3 × 8 decoders

4-to-1-Line Multiplexer



(a) Logic diagram

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table