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PPT ON COMBINATIONAL CIRCUIT FOR CODE CONVERTERS

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Functional Blocks

- Fundamental circuits that are the base building blocks of most larger digital circuits
- They are reusable and are common to many systems.
- Examples of functional logic circuits
  - Decoders
  - Encoders
  - Code converters
  - Multiplexers

Where they are used

- Multiplexers
  - Selectors for routing data to the processor, memory, I/O
  - Multiplexers route the data to the correct bus or port.
- Decoders
  - are used for selecting things like a bank of memory and then the address within the bank. This is also the function needed to 'decode' the instruction to determine the operation to perform.
- Encoders
  - are used in various components such as keyboards.

Formulation step

- Convert the specifications into a variety forms for optimal implementation.
  - Possible forms
    - Truth Tables
    - Expressions
    - K-maps
    - Binary Decision Diagrams

Last 3 steps

- Best illustrated by example
  - A BCD to Excess-3 code converter

BCD-to-Excess-3 Code converter

- BCD is a code for the decimal digits 0-9
- Excess-3 is also a code for the decimal digits

Decimal Digit	Input BCD	Output Excess-3
0	0 0 0 0	0 0 1 1
1	0 0 0 1	0 1 0 0
2	0 0 1 0	0 1 0 1
3	0 0 1 1	0 1 1 0
4	0 1 0 0	0 1 1 1
5	0 1 0 1	1 0 0 0
6	0 1 1 0	1 0 0 1
7	0 1 1 1	1 0 1 0
8	1 0 0 0	1 0 1 1
9	1 0 0 1	1 1 0 0

Specification of BCD-to-Excess3

- Inputs: a BCD input, A,B,C,D with A as the most significant bit and D as the least significant bit.
- Outputs: an Excess-3 output W,X,Y,Z that corresponds to the BCD input.
- Internal operation – circuit to do the conversion in combinational logic.

Formulation of BCD-to-Excess-3

- Excess-3 code is easily formed by adding a binary 3 to the binary or BCD for the digit.
- There are 16 possible inputs for both BCD and Excess-3.
- It can be assumed that only valid BCD inputs will appear so the six combinations not used can be treated as don't cares.

Expressions for W X Y Z

- $W(A,B,C,D) = \Sigma m(5,6,7,8,9) + d(10,11,12,13,14,15)$
- $X(A,B,C,D) = \Sigma m(1,2,3,4,9) + d(10,11,12,13,14,15)$
- $Y(A,B,C,D) = \Sigma m(0,3,4,7,8) + d(10,11,12,13,14,15)$
- $Z(A,B,C,D) = \Sigma m(0,2,4,6,8) + d(10,11,12,13,14,15)$

Two level circuit implementation

- Have equations
  - W = A + BC + BD = A + B(C+D)
  - X = B'C + B'D + BC'D' = B'(C+D) + BC'D'
  - Y = CD + C'D'
  - Z = D'
- Factoring out (C+D) and call it T
- Then T' = (C+D)' = C'D'
  - W = A + BT
  - X = B'T + BT'
  - Y = CD + T'
  - Z = D'

Create the digital circuit

- Implementing the second set of equations where T=C+D results in a lower gate count.
- This gate has a fanout of 3