JYOTHISHMATHI INSTITUTE OF TECHNOLOGY & SCIENCE

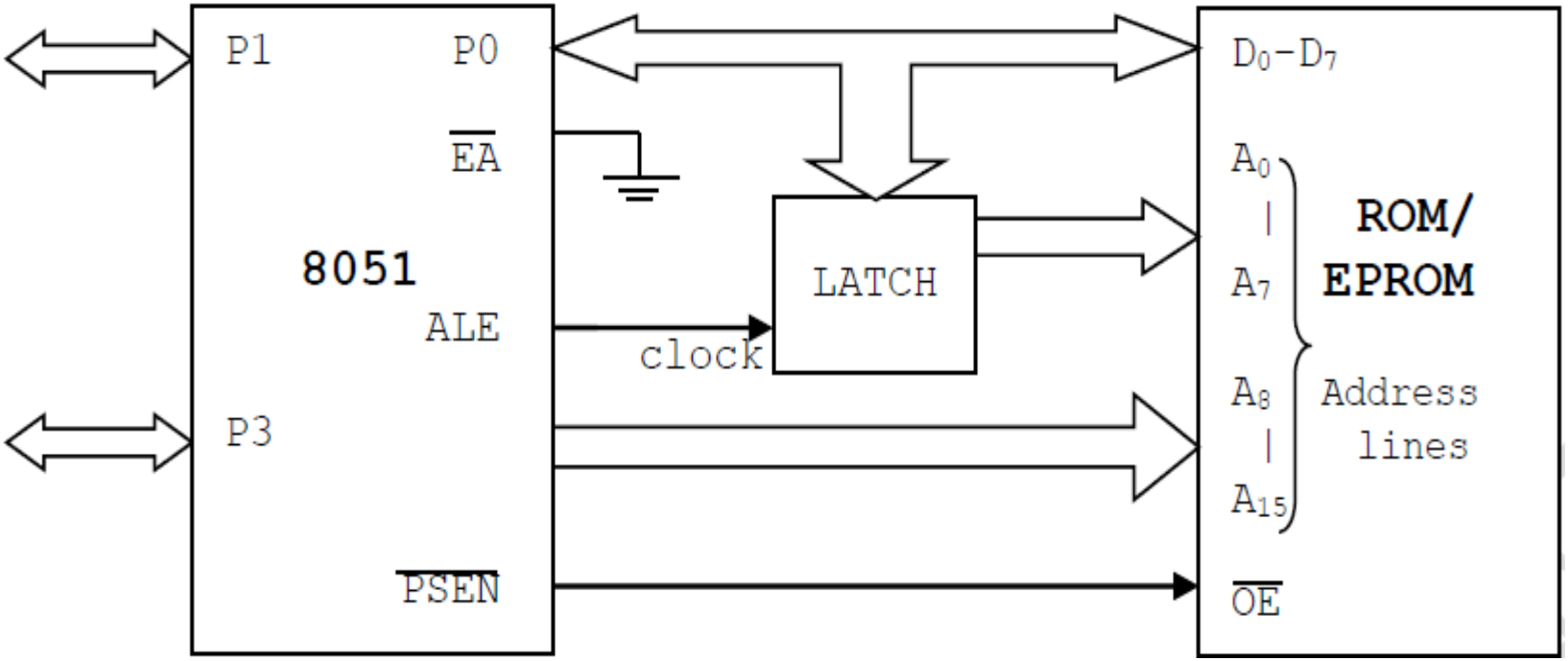
MICRO PROCESSORS & MICRO CONTROLLERS

MEMORY INTERFACING

D. Pushpalatha

MEMORY INTERFACING

ROM Interfacing



ROM Interfacing

- Port 0 : Is used as multiplexed data & adress lines it gives lower order (A_7- A_0) 8 bit address in initial T cycles and higher order (A_8- A_{15}) used as data bus.
- 8 bit address is latched using external latch & ALE signal from 8051.

ROM Interfacing

- Port 2 : provides higher order (A_{15}- A_8) 8 bit address.

  PSEN' is used to activate the output enable signal of external ROM/EPROM.

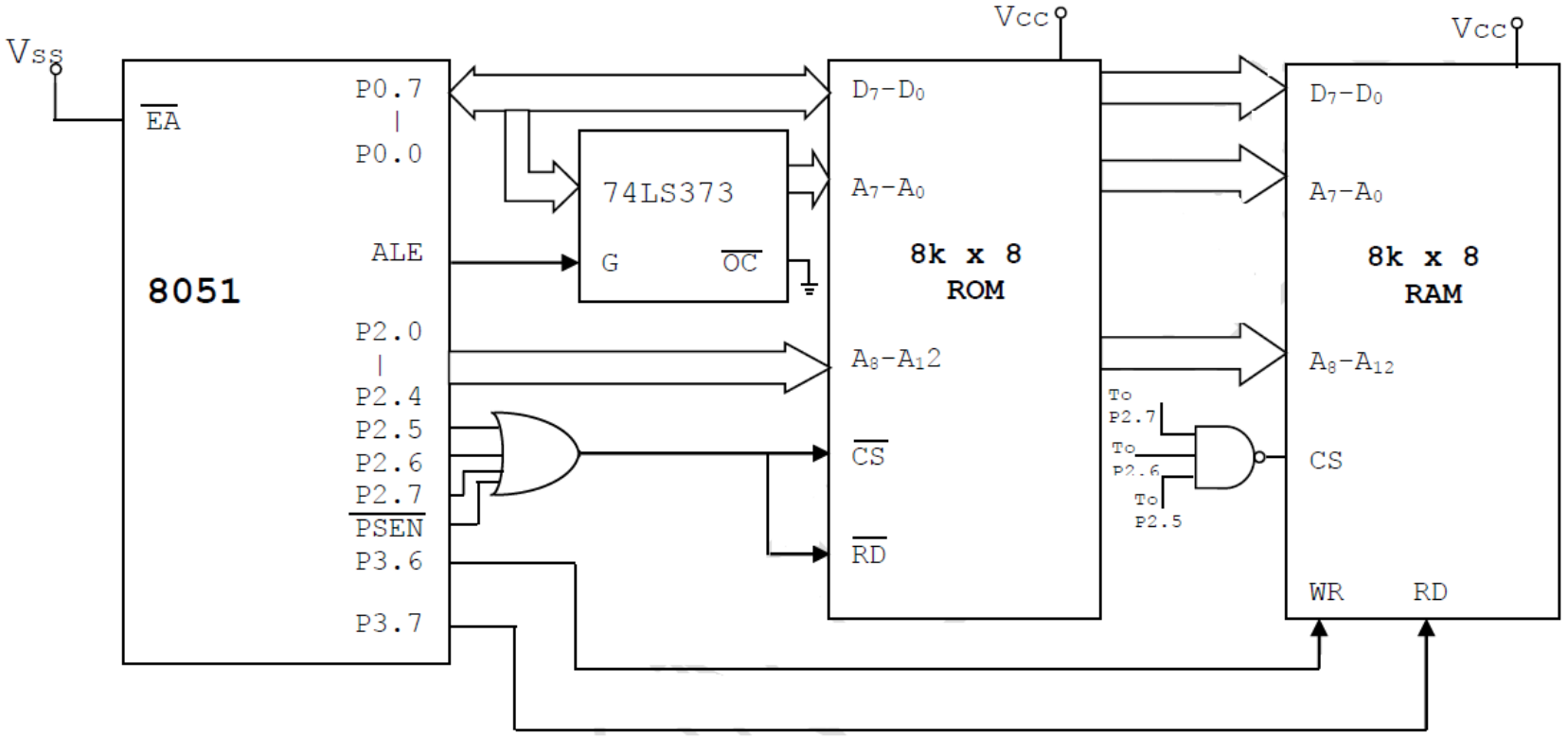
Address Decoding (Memory Map) for 8k x 8 ROM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFH

Address Decoding (Memory Map) for 8k x 8 RAM.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	E000H
end	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFH

8k x 8k ROM


Vss
EA
P0.7
|
P0.0
ALE
8051
P2.0
|
P2.4
P2.5
P2.6
P2.7
PSEN
P3.6
P3.7
74LS373
G
OC
Vcc
D7-D0
A7-A0
8k x 8
ROM
A8-A12
CS
RD
To
P2.7
To
P2.6
To
P2.5
Vcc
D7-D0
A7-A0
8k x 8
RAM
A8-A12
CS
WR
RD