## JYOTHISHMATHI INSTITUTE OF TECHNOLOGY & SCIENCE



#### MICRO PROCESSORS & MICRO CONTROLLERS

Department of ECE Jyothishmathi Institute of Technology

### Random Access Memory



Static Random Access Memory (SRAM)

### Random Access Memory



#### k-bit address

- Decoder requires 2<sup>k</sup> AND gates
  - Each AND gate has k inputs
- For large k this becomes prohibitive.
- Use <u>2-dimensional decoding</u>
  - Two decoders
  - Each decoder requires 2<sup>(k/2)</sup> AND gates
    - Each AND gate has k/2 inputs
  - Far less combinational logic



- The size of a chip package is often dictated by the number of input and output signals.
- For large memories, the number of address lines often becomes prohibitive.
- Use <u>address multiplexing</u>
  - The same address lines are used both for the row address and the column address
  - Use time multiplexing to first latch the row address and then latch the column address



# **RAM Systems**

- Often RAM chips are smaller than the required memory size.
- What if you need a wider memory?
   Larger word size
- What if you need a deeper memory?
  - Greater number of memory locations

- ROM store "permanent" binary information
  - One-time programmable memory
  - Multiple-time programmable memory
- Address and Data
  - k address bits
  - n data bits
- 2<sup>k</sup> x n ROM includes
  - k-to-2<sup>k</sup> decoder
  - n 2<sup>k</sup>-input OR gates





#### Table 7.3 ROM Truth Table (Partial)

Inputs					Outputs							
<b>I</b> 4	I <sub>3</sub>	<b>I</b> 2	<i>I</i> 1	I <sub>0</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	<b>A</b> 1	A <sub>0</sub>
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		÷										
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1



- EEPROM (E<sup>2</sup>PROM)
  - Electrically Erasable Programmable ROM
- Flash ROM
  - Similar to E<sup>2</sup>PROM
  - Has additional circuitry to selectively erase and program the memory in-circuit
  - Does not require a special programmer

#### Programmable Logic Devices

# Programmable Logic Devices

- Programmable Logic Arrays (PLA)
- Programmable Array Logic (PAL)
- Simple Programmable Logic Device (SPLD)
- Complex Programmable Logic Device (CPLD)
- Field Programmable Gate Array (FPGA)