OPAMPS

N.Raju
Associate Professor
ECE
Jyothishmathi Institute of Technology & Science

Sequential Circuits

Every digital system is likely to have combinational circuits, most systems encountered in practice also include storage elements, which require that the system be described in term of sequential logic.

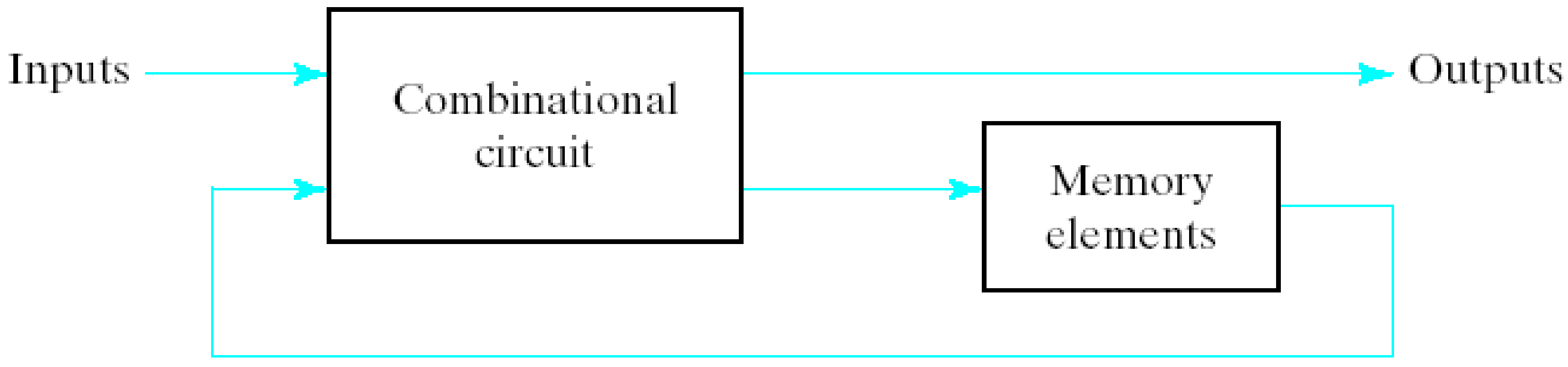


Fig. 5-1 Block Diagram of Sequential Circuit

Synchronous Clocked Sequential Circuit

A sequential circuit may use many flip-flops to store as many bits as necessary. The outputs can come either from the combinational circuit or from the flip-flops or both.

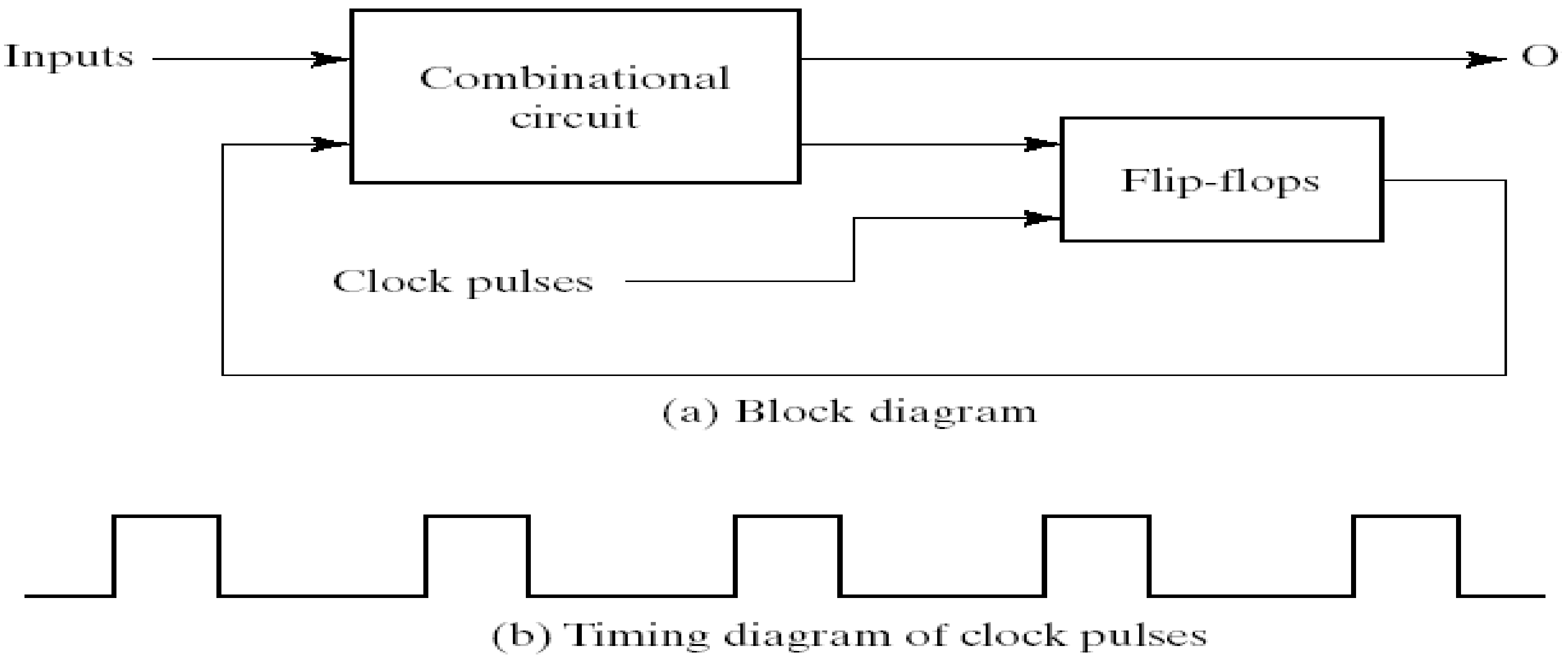
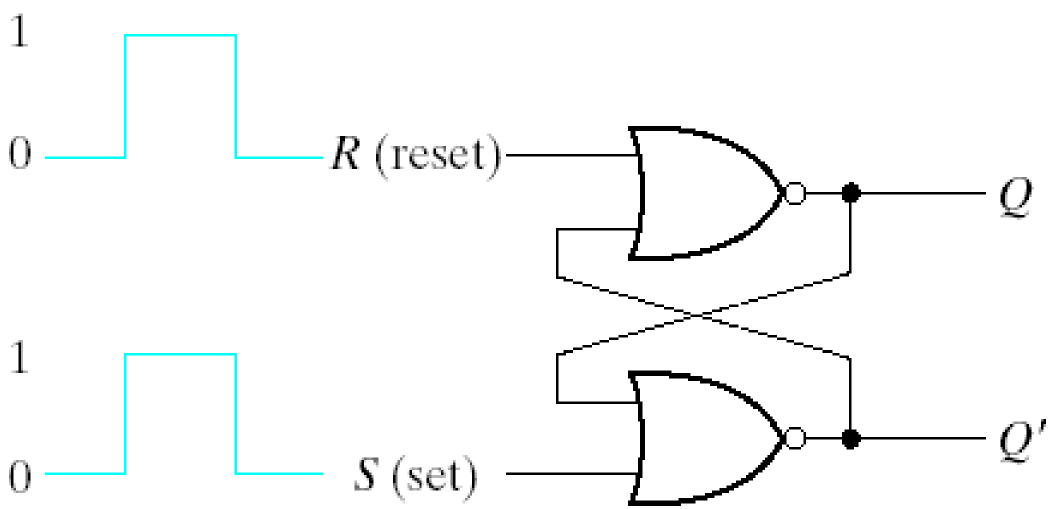


Fig. 5-2 Synchronous Clocked Sequential Circuit

Latches SR Latch

The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates. It has two inputs labeled S for set and R for reset.



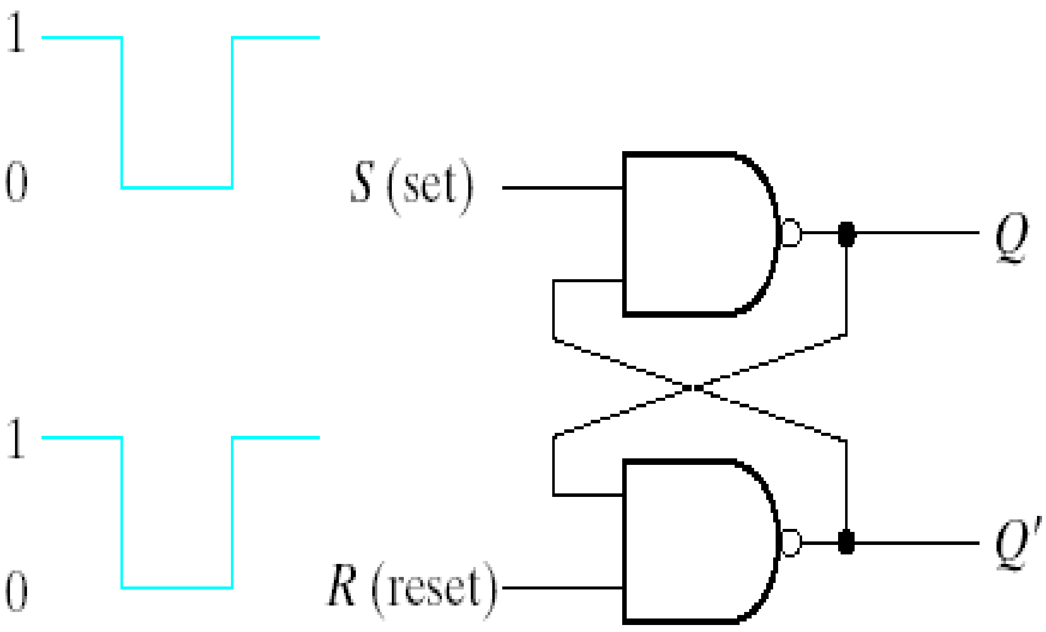
(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(b) Function table

Fig. 5-3 *SR* Latch with NOR Gates

SR Latch with NAND Gates



(a) Logic diagram

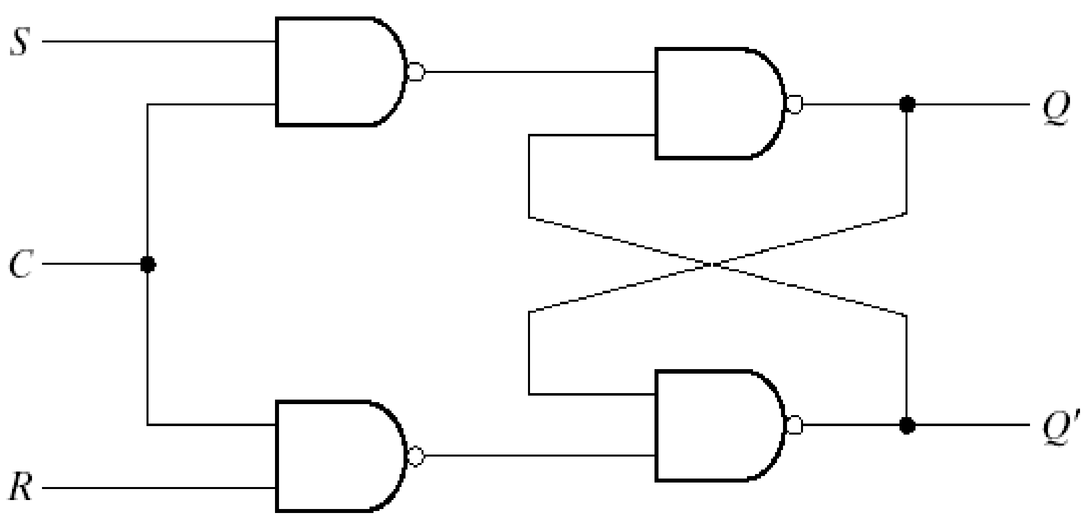
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(b) Function table

Fig. 5-4 *SR* Latch with NAND Gates

SR Latch with Control Input

The operation of the basic SR latch can be modified by providing an additional control input that determines when the state of the latch can be changed. In Fig. 5-5, it consists of the basic SR latch and two additional NAND gates.



(a) Logic diagram

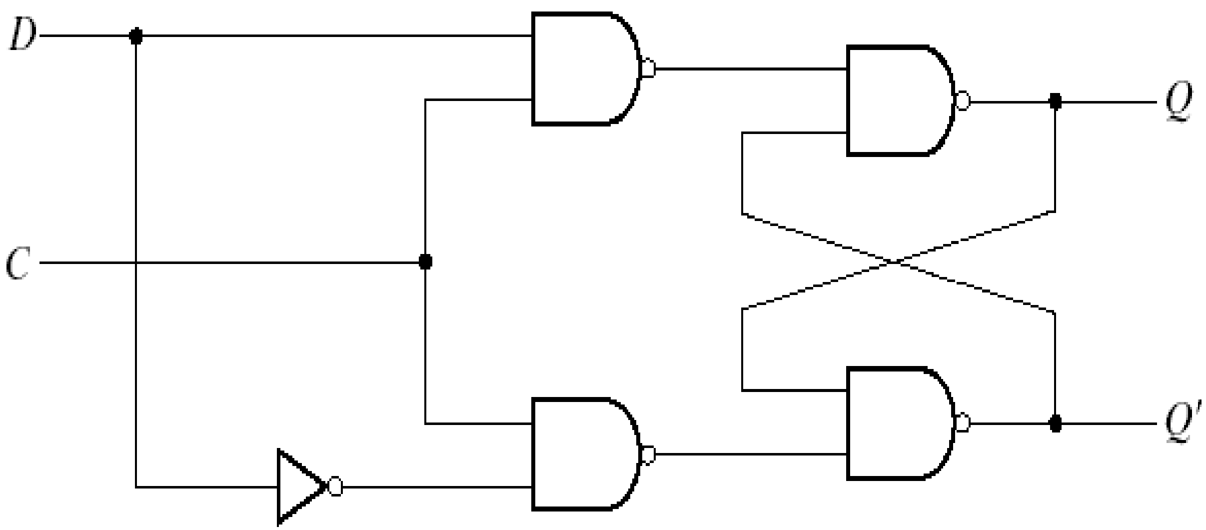
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

D Latch

One way to eliminate the undesirable condition of the indeterminate state in SR latch is to ensure that inputs S and R are never equal to 1 at the same time in Fig 5-5. This is done in the D latch.



(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

(b) Function table

Fig. 5-6 D Latch

Graphic Symbols for latches

A latch is designated by a rectangular block with inputs on the left and outputs on the right. One output designates the normal output, and the other designates the complement output.

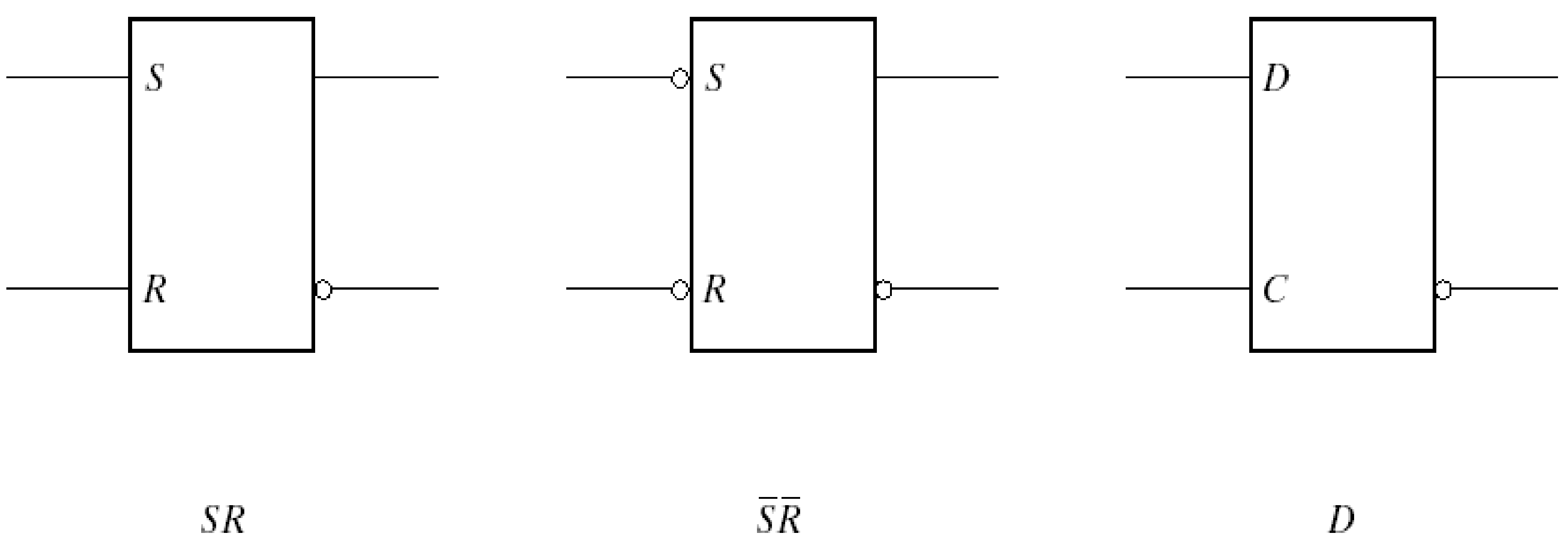


Fig. 5-7 Graphic Symbols for Latches

Flip-Flops

The state of a latch or flip-flop is switched by a change in the control input. This momentary change is called a trigger and the transition it cause is said to trigger the flip-flop. The D latch with pulses in its control input is essentially a flip-flop that is triggered every time the pulse goes to the logic 1 level. As long as the pulse input remains in the level, any changes in the data input will change the output and the state of the latch.

Clock Response in Latch

In Fig (a) a positive level response in the control input allows changes, in the output when the D input changes while the clock pulse stays at logic 1.

(a) Response to positive level

Clock Response in Flip-Flop

(b) Positive-edge response

(c) Negative-edge response

Edge-Triggered D Flip-Flop

The first latch is called the master and the second the slave. The circuit samples the D input and changes its output Q only at the negative-edge of the controlling clock.

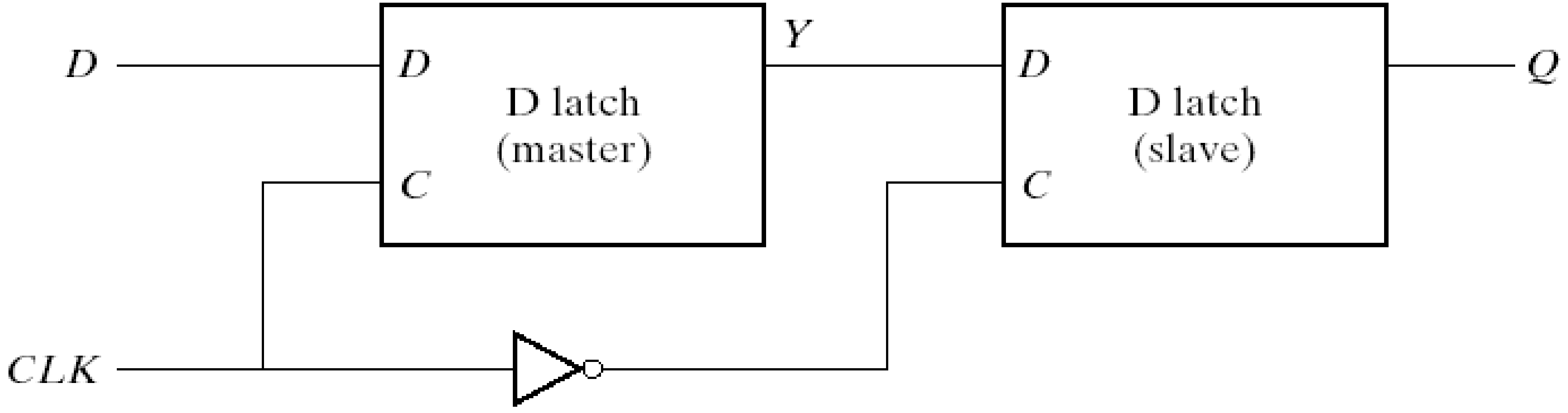


Fig. 5-9 Master-Slave *D* Flip-Flop

D-Type Positive-Edge-Triggered Flip-Flop

Another more efficient construction of an edge-triggered D flip-flop uses three SR latches. Two latches respond to the external D(data) and CLK(clock) inputs. The third latch provides the outputs for the flip-flop.

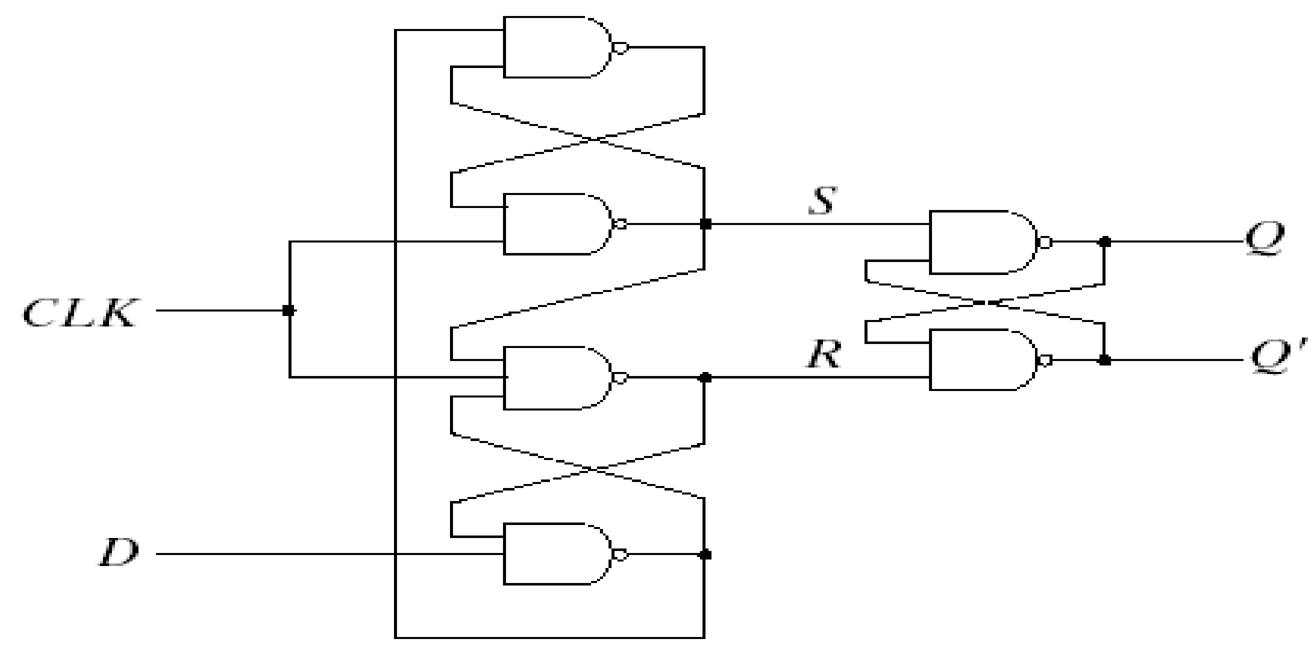


Fig. 5-10 *D*-Type Positive-Edge-Triggered Flip-Flop

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Graphic Symbol for Edge-Triggered D Flip-Flop

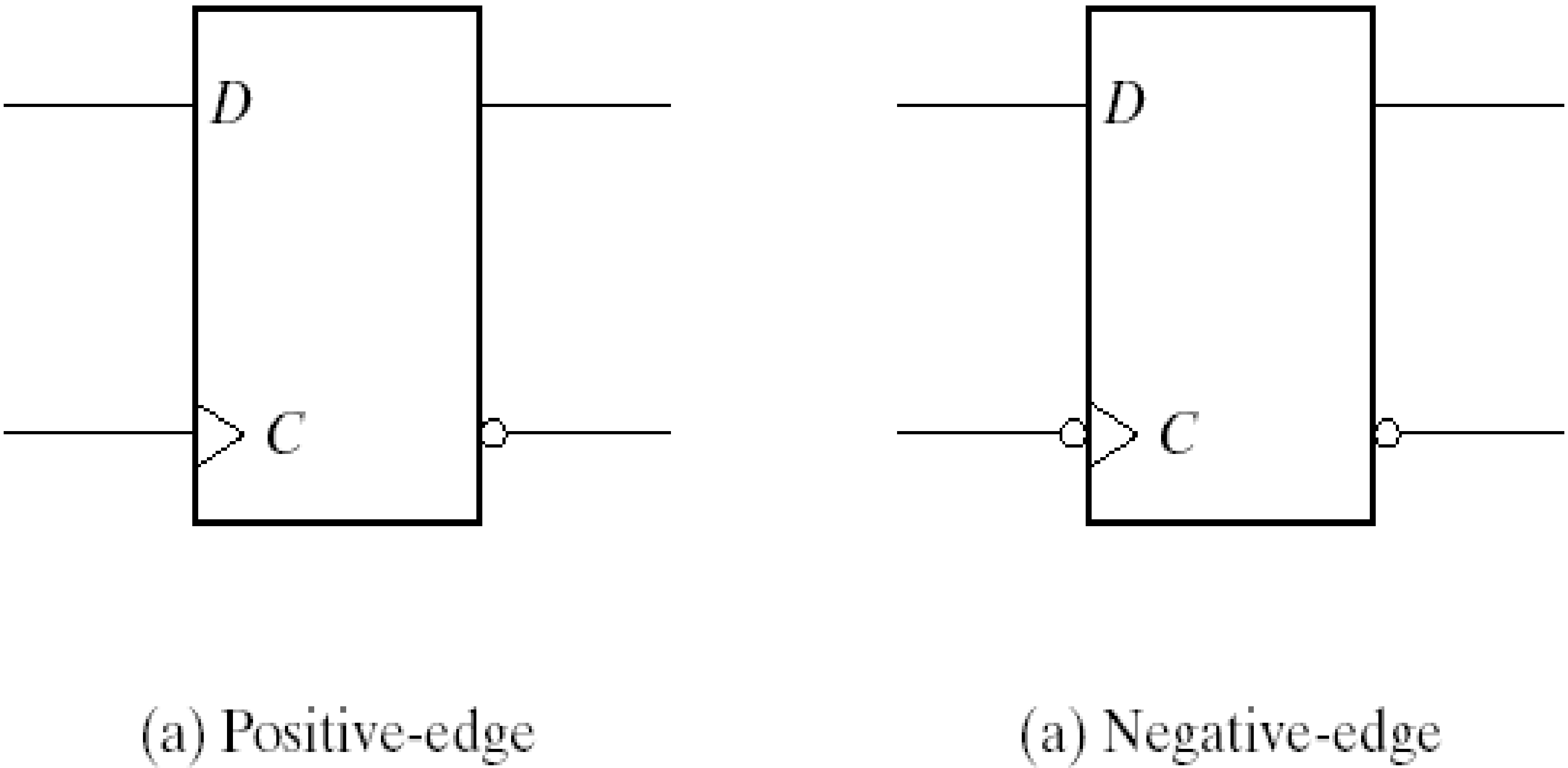
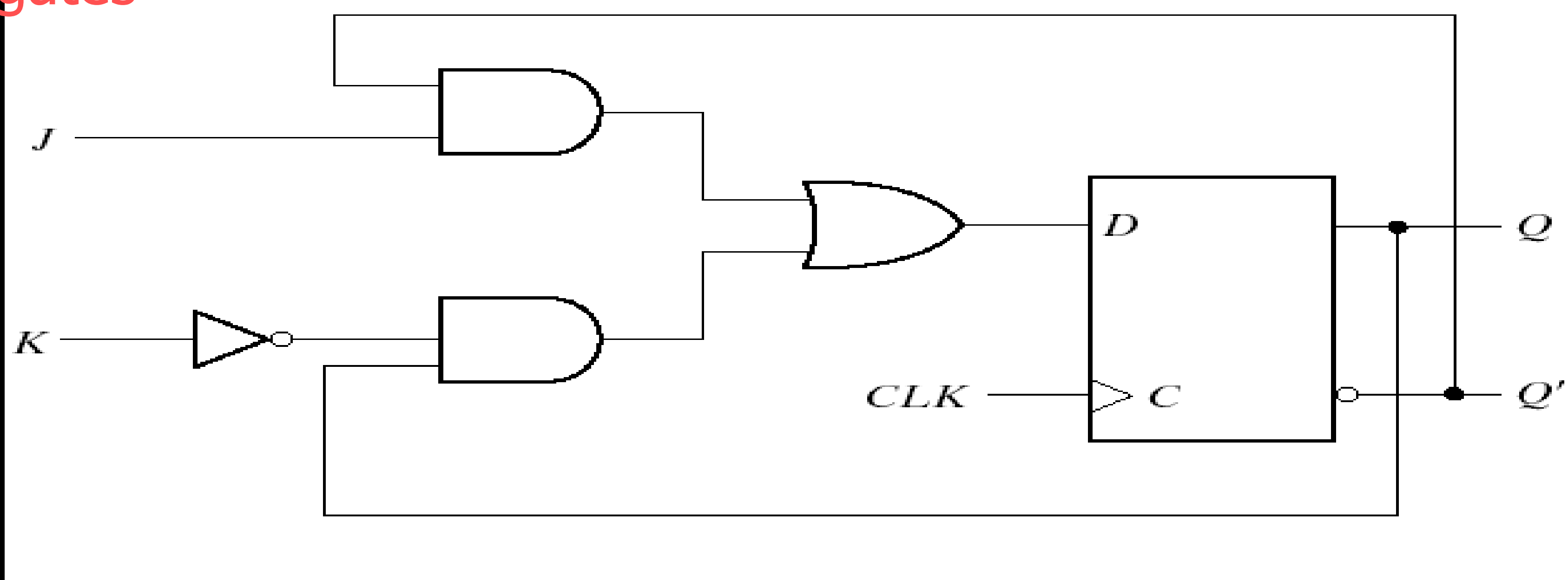


Fig. 5-11 Graphic Symbol for Edge-Triggered *D* Flip-Flop

Other Flip-Flops JK Flip-Flop

There are three operations that can be performed with a flip-flop: set it to 1, reset it to 0, or complement its output. The JK flip-flop performs all three operations. The circuit diagram of a JK flip-flop constructed with a D flip-flop and gates

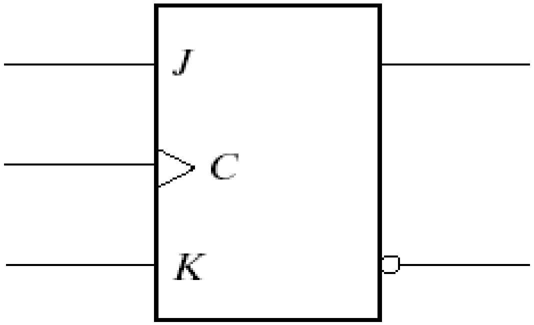


(a) Circuit diagram

JK Flip-Flop

The J input sets the flip-flop to 1, the K input resets it to 0, and when both inputs are enabled, the output is complemented. This can be verified by investigating the circuit applied to the D input:

$$D = J Q` + K` Q$$



(b) Graphic symbol

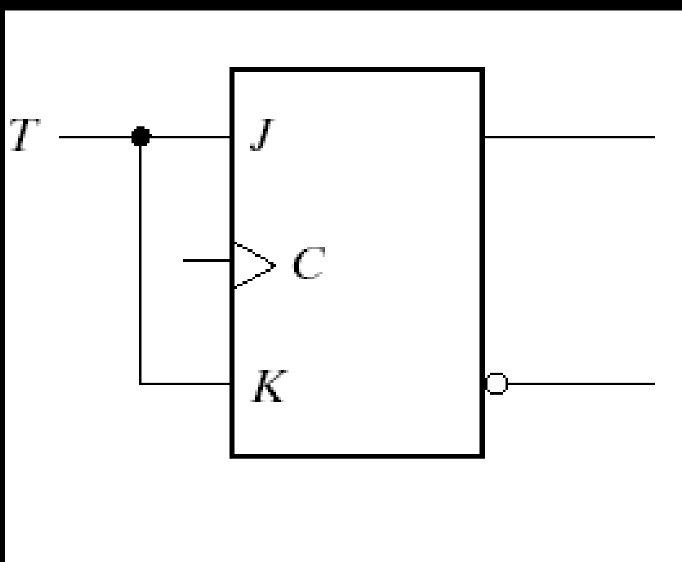
Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	$Q(t+1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

T Flip-Flop

The T(toggle) flip-flop is a complementing flip-flop and can be obtained from a JK flip-flop when inputs J and K are tied together.



(a) From *JK* flip-flop

D Flip-Flop

D	$Q(t+1)$	
0	0	Reset
1	1	Set

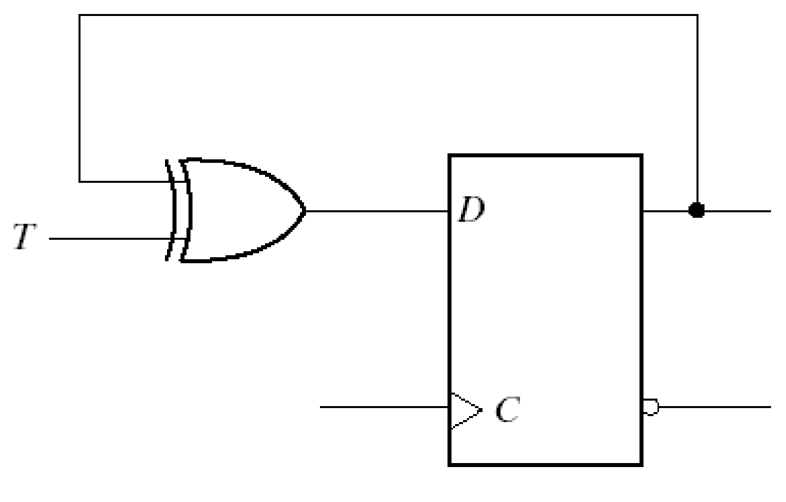
T Flip-Flop

T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

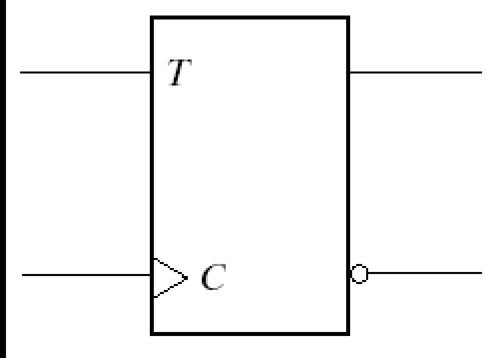
T Flip-Flop

The T flip-flop can be constructed with a D flip-flop and an exclusive-OR gates as shown in Fig. (b). The expression for the D input is

$$D = T \oplus Q = TQ` + T`Q$$



(b) From *D* flip-flop



(c) Graphic symbol

Characteristic Equations

D flip-flop Characteristic Equations

$$Q(t+1) = D$$

JK flip-flop Characteristic Equations

$$Q(t+1) = JQ` + K`Q$$

T flip-flop Characteristic Equations

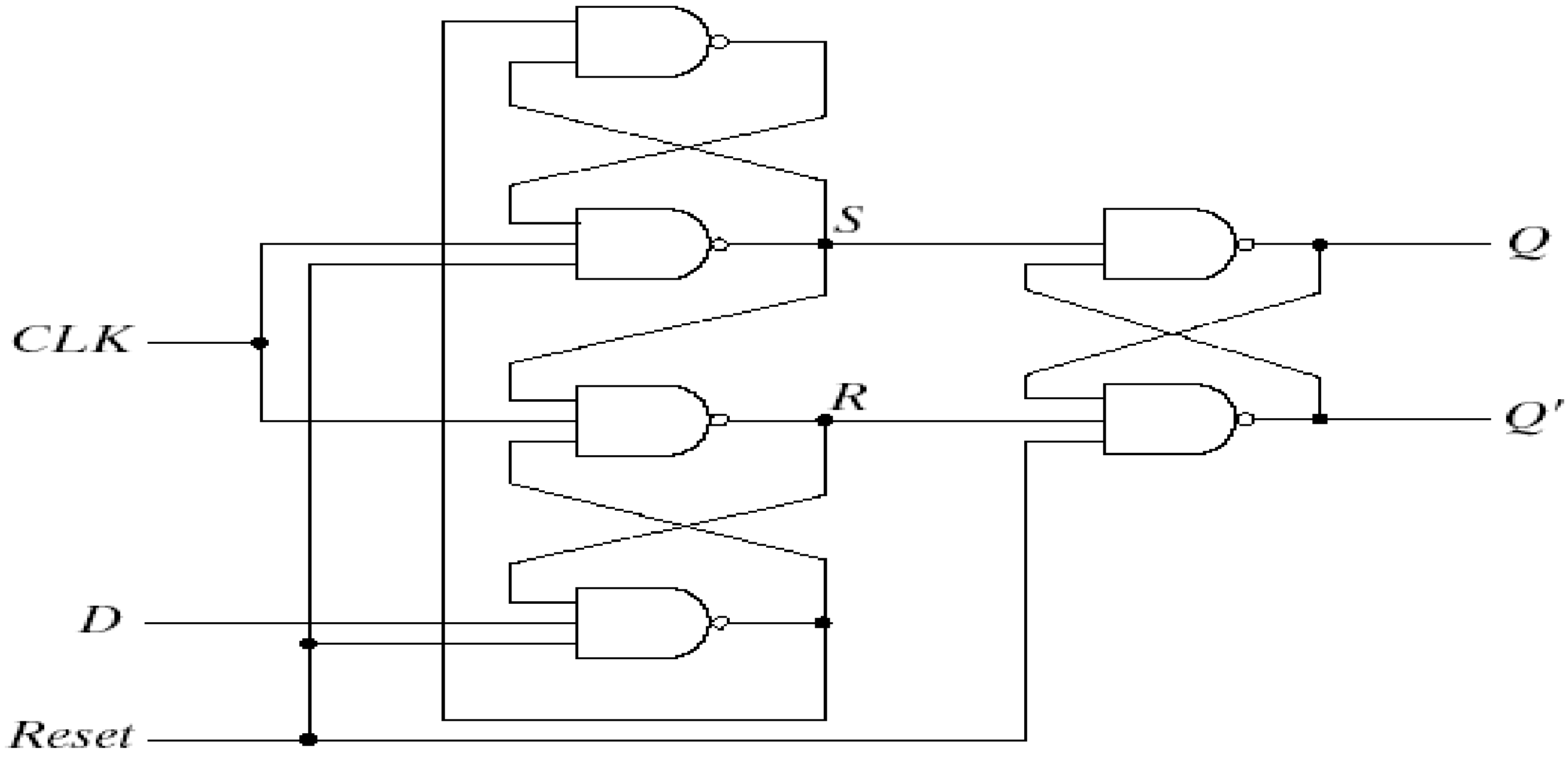
$$Q(t+1) = T \oplus Q = TQ` + T`Q$$

Direct Inputs

Some flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state independent of the clock. The input that sets the flip-flop to 1 is called present or direct set. The input that clears the flip-flop to 0 is called clear or direct reset. When power is turned on a digital system, the state of the flip-flops is unknown. The direct inputs are useful for bringing all flip-flops in the system to a known starting state prior to the clocked operation.

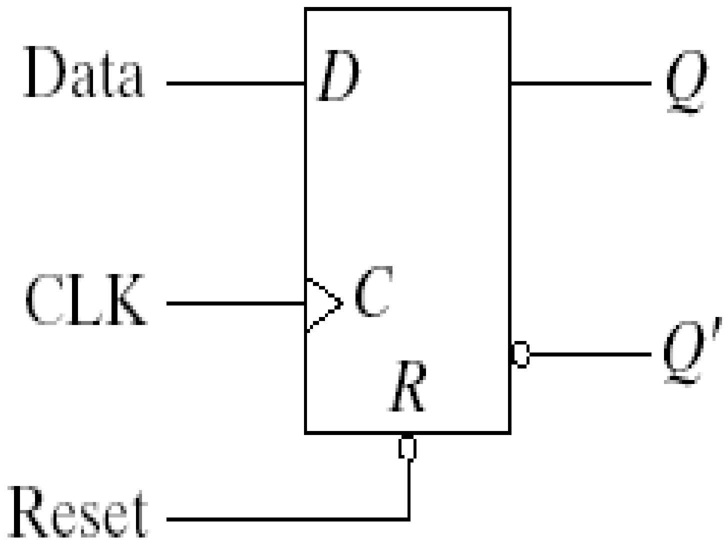
D Flip-Flop with Asynchronous Reset

A positive-edge-triggered D flip-flop with asynchronous reset is shown in Fig(a).



(a) Circuit diagram

D Flip-Flop with Asynchronous Reset



(b) Graphic symbol

R	C	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table