JYOTHISHMATHI INSTITUTE OF TECHNOLOGY & SCIENCE

(An ISO 9001: 2015 Certified Institution)

Approved by AICTE and Affiliated to JNTUH Hyderabad

IEEE MADRAS SECTION

One week FDP on

Hands on Training on ANSYS HFSS and CADENCE TOOL

Organized by

Research and Development Centre

&

Department of Electronics and Communication Engineering

15th February 2021 to 20th February 2021

About the FDP:

This FDP aiming at bringing together researchers from academia and industry on various cutting-edge research areas Antenna, Antenna Arrays, Optimization, Communications, Smart Antennas to create awareness about these domains. The workshop will include sessions focused on technologies, techniques and applications with intent to foster the exchange of knowledge and ideas between experts. The objective of the course is to impart in-depth knowledge in the Computer-aided design of antennas through MATLAB and EM simulators. The workshop provides hands-on experience in using ANSYS HFSS simulator tools, leading to the design of patch antennas and other types of antennas. 6-day programme will enable the participants to understand the

ANSYS HFSS

CADENCE TOOL

This FDP is intended for young faculty members working in engineering colleges and research scholars to make them familiar with latest trends in VLSI Design/Technology and to enrich them with depth and breadth of knowledge. In VLSI design, the methodology makes extensive use of CAD techniques for all the tasks that span design through layout to finally "sign-off the design database" for chip fabrication. In addition to theoretical knowledge, the aim of this FDP is to equip the participants with hands-on experience in the state-of-art Cadence tools for VLSI Design supporting Analog and Digital Front End and Back End.

Major Course Contents:

- Fundamentals of Electromagnetic and Antenna Theory
- Introduction to Advanced Antenna Arrays
- Introduction to Soft computing /Evolutionary (Numerical and optimization)
- Algorithms methods in antenna design Miniaturization of antenna array
- HFSS/CST Simulation and Basis Demonstrations
- Hands on design labs using HFSS simulator
- Reconfigurable Antennas Multiple beam and beam forming antennas
- Antenna in IOT
- Antenna interactions and coupling analysis
- Antenna design using HFSS- Hands on session
- Reconfigurable and multi beam antennas/arrays

Topics Covered

1. Overview of VLSI Design Flow, Tools and Methodology; System Architecture Design.
2. Latest trends in ASIC Design, Design for Verification, DFT, Constraint driven Synthesis, STA
3. Physical Design, Timing Driven P&R, Physical Verification, DFM etc.
4. Challenges involved in design of Digital/Analog/Mixed Signal circuits for IP and System on Chip (SoC).
5. Analog Design Modeling using Verilog-A and Simulation; Analog IC Design using Cadence Virtuoso; Lab Sessions on Verilog-AMS.
6. Emerging Applications of VLSI in IoT, Artificial Intelligence, DSP, Wireless Communications etc.
7. Opportunities for Research in VLSI Design.

Contact Person:
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Certification:

Certificates will be issued to the participants who have a minimum of 80% attendance.

No registration Fee

Registration to be done on or before **12/02/2021**

Confirmation of participation will be sent through email on or before **13/02/2021.**