



# **Ring counter & twisted ring counter**

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**AIM :** To construct a ring counter & twisted ring counter using 4 Bit shift register.

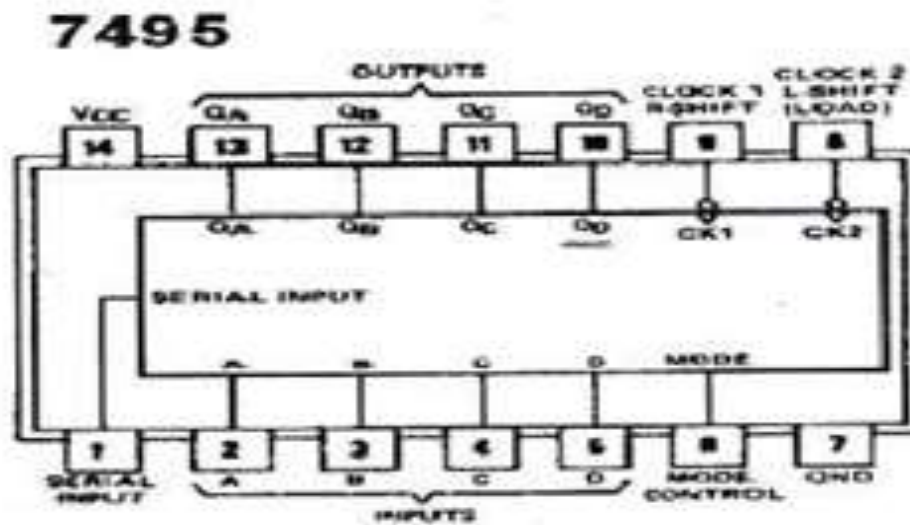
**APPARATUS:**

1. Physitech ring counter & twisted ring counter using 4 Bits shift register trainer kit.
2. Patch cards.

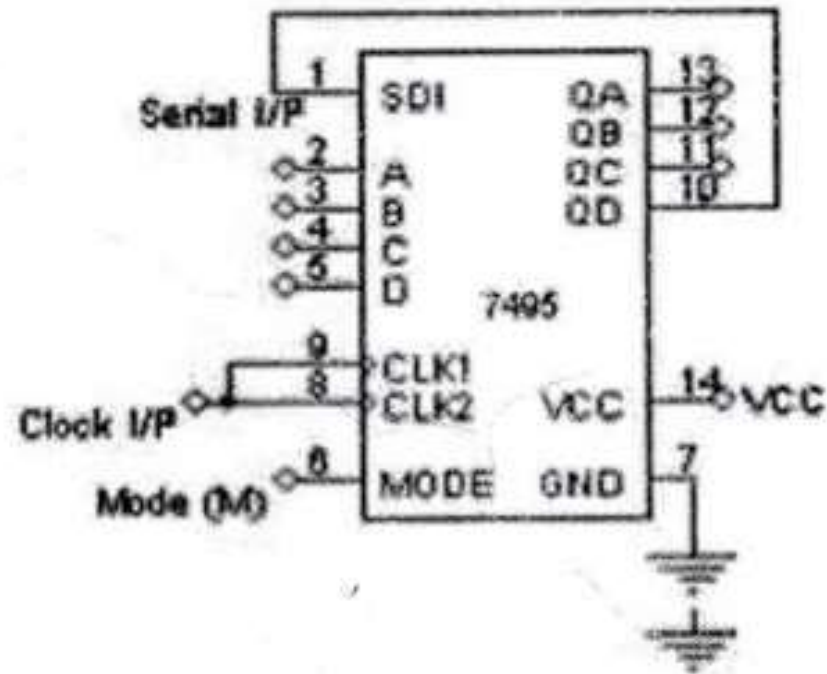
**THOERY:**

Ring counter is basic register with direct feedback such that the contents of the register simply circulate around the register when the clock is running .Here the last output that is QD in a shift register is connected back to the serial input.A basic ring counter can be slightly modified to produce another type of shift register counter called Jhonson counter .Here complement of last output is connected back to the not gate input and not gate output is connected back to serial input.A four bit Jhonson counter gives 8 state output.

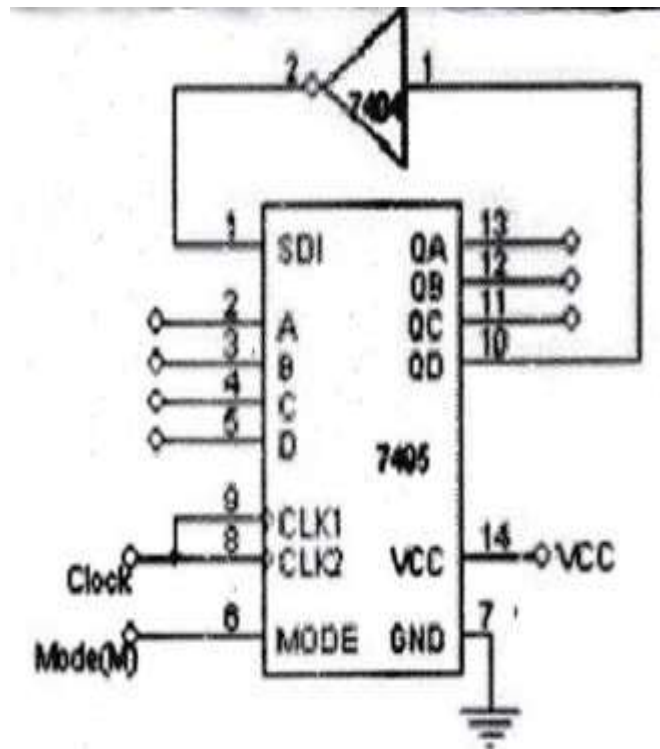
Pin diagram:



**CIRCUIT DIAGRAM:  
RING COUNTER:**



## TWISTED RING COUNTER:



## **PROCEDURE:**

### **Ring counter:**

1. Make the connection as show in the ring counter circuit diagram.
2. connect the inputs A,B,C,D to input switch present on trainer kit.
3. connect the outputs QA,QB,QC,QD.
4. connect the serial input to pin 10 of the 7495 IC i.e., QD.
5. connect 8<sup>th</sup> & 9<sup>th</sup> pin's of the IC 7495 to clock, which is present on the trainer kit.
6. connect mode(M) 6<sup>th</sup> pin of IC 7495 to input switch.
7. Verify the truth table of ring counter.

**Twisted ring counter:**

1. Make the connection as show in the twisted ring counter circuit diagram.
- 2.connect the inputs A,B,C,D to input switch present on trainer kit.
- 3.connect the outputs QA,QB,QC,QD.
4. connect the serial input to NOT gate , clock,which is present on the trainer kit.
- 5.connect the terminal of the NOT Gate pin 10 of the IC 7495 i.e, QD.
- 6.connect the 8<sup>th</sup> & 9<sup>th</sup> pin's of the IC 7495 to clock ,which is present on the trainer kit.
6. connect mode(M) 6<sup>th</sup> pin of IC 7495 to input switch.
- 7.Verify the truth table of twisted ring counter.



**Truth table:**

**Ring counter:**

Set the mode to HIGH and LOW condition for reset.

Clock	QA	QB	QC	QD
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1
8	1	0	0	0

## Twisted ring counter:

Clock	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0



**Result:** verified the truth table of ring counter & twisted ring counter using 4 Bit shift register

**THANK YOU**