**JYOTHISHMATHI INSTITUTE OF TECHNOLOGY & SCIENCE**
**UGC AUTONOMOUS Institution**
Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
(Accredited with NAAC 'A' Grade | ISO 9001:2015 Certified
UG - CSE,ECE,EEE Accredited by National Board of Accreditation, New Delhi)

Date: 05-08-2023

AY: 2022-23

# END EXAMINATION TIME TABLE
## I-M.TECH-II-SEM..J-22 REGULATION REGULAR EXAMINATIONS-AUGUST-2023

| DATE | VLSI SYSTEM DESIGN | COMPUTEER SCIENCE AND ENGINEERING | Examination Timings |
|---|---|---|---|
| 14-08-2023 Monday | VLSI Advanced Physical Design | Advanced Algorithms | 10-00 AM To 01-00 PM |
| 16-08-2023 Wednesday | System Verilog Test Benches Using UVM | Advanced Computer Architecture | |
| 18-08-2023 Friday | Design for Testability (PE-III) | Advanced Computer Networks (PE-III) | |
| 21-08-2023 Monday | Device Modeling (PE-IV) | Nature Inspired Computing (PE-IV) | |

5/8/23 Controller of Exams

5/8/23 DEAN-Exams

7/8/23 PRINCIPAL

Copy to:

1. Chairman Garu
2. Secretary Garu
3. DEAN-(Student affairs)
4. Website Co-ordinator
5. All HODS
6. Supdt.
7. Office-Accounts Section.
8. Notice board
9. File.